

FIG. 1

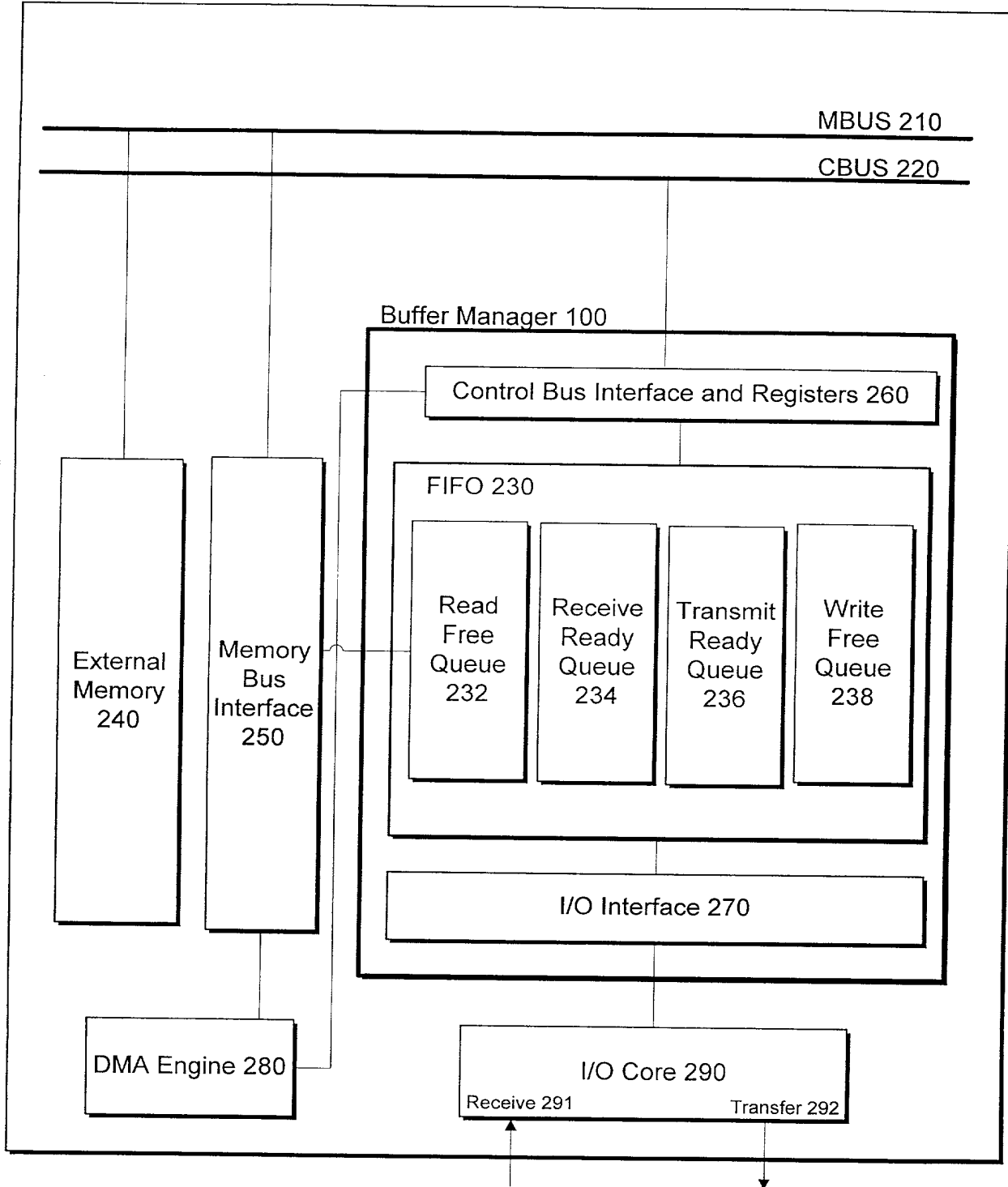


FIG. 2

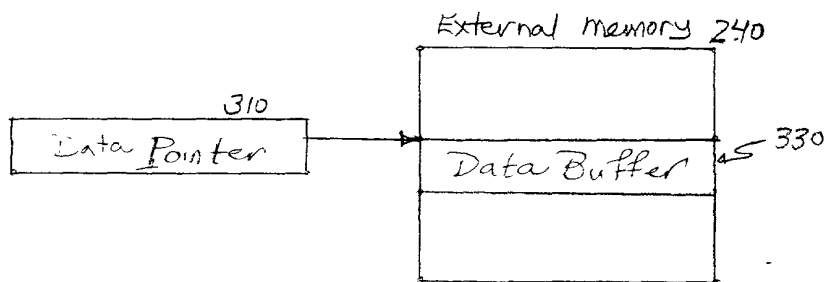


FIG. 3A

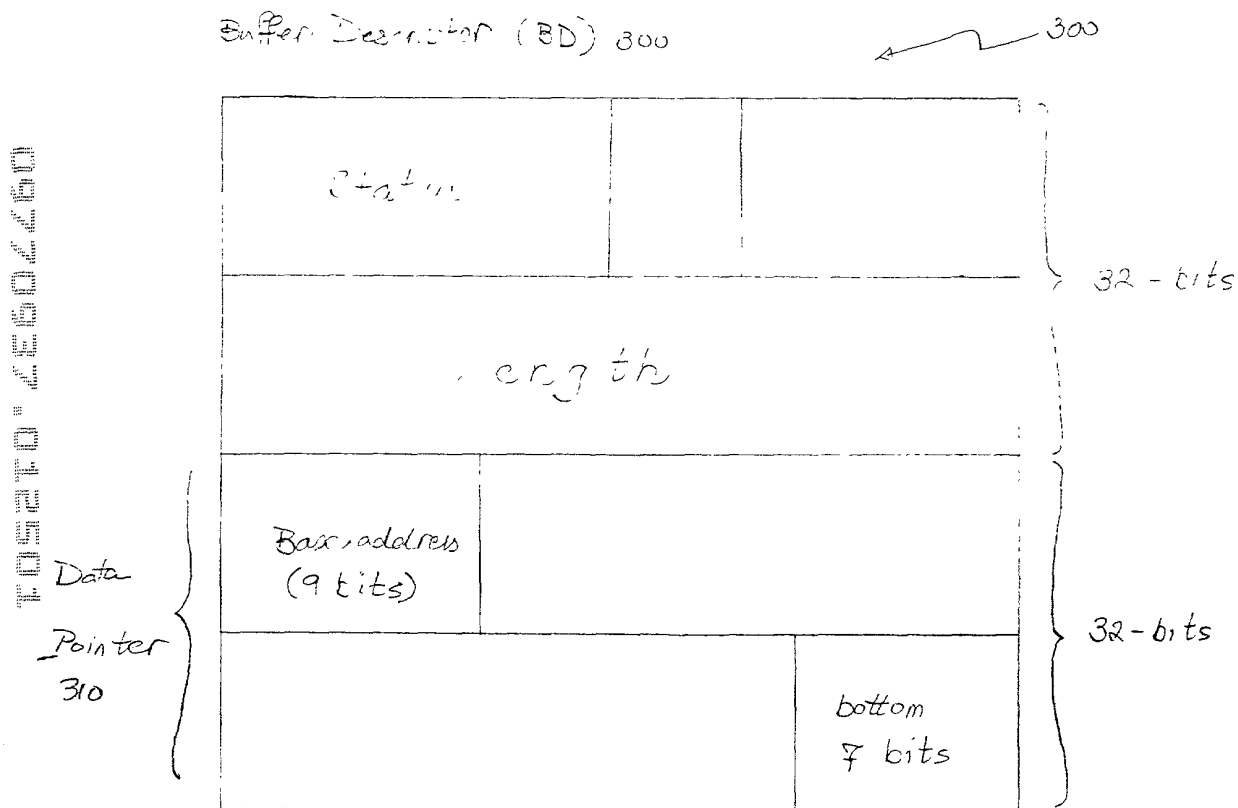


FIG. 3B

Configuration	Bit 8	Bit 7	Transmit Queue #	Depth
1	0	0	1-4	32
2	0	1	1-2	40
			3-4	24
3	1	0	1	80
			2-3	24
			4	0
4	1	1	1	64
			2	64
			3	0
			4	0

Transmit Ready Queue Configuration

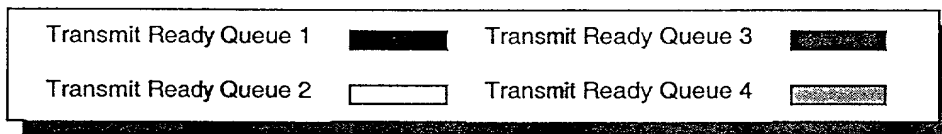


FIG. 4

09770597.01901
T09270.2E50260

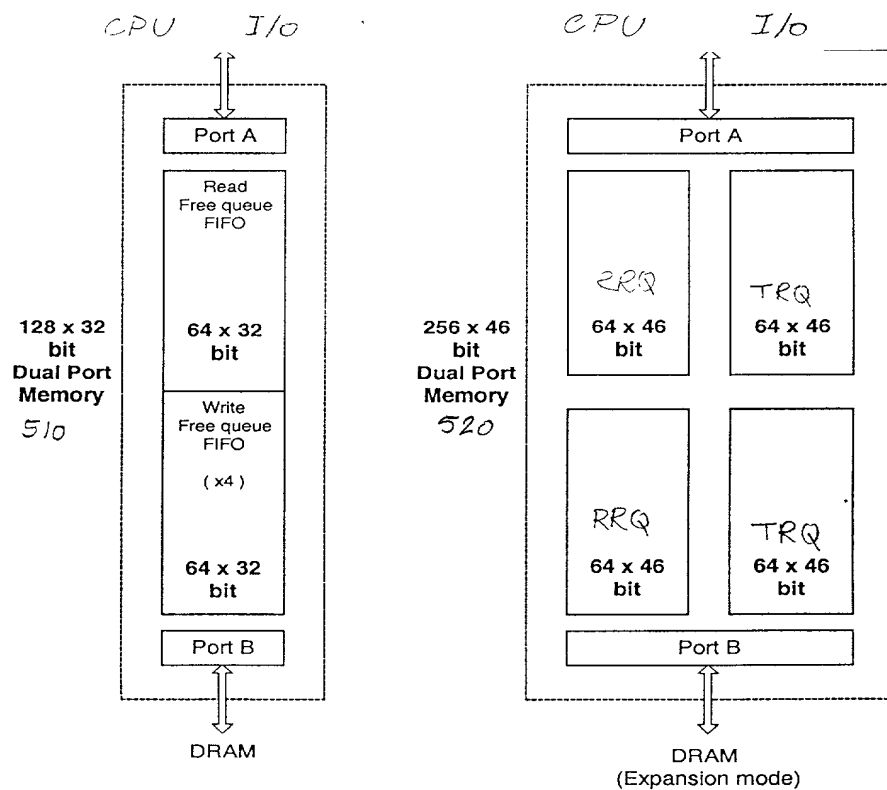


FIG. 5

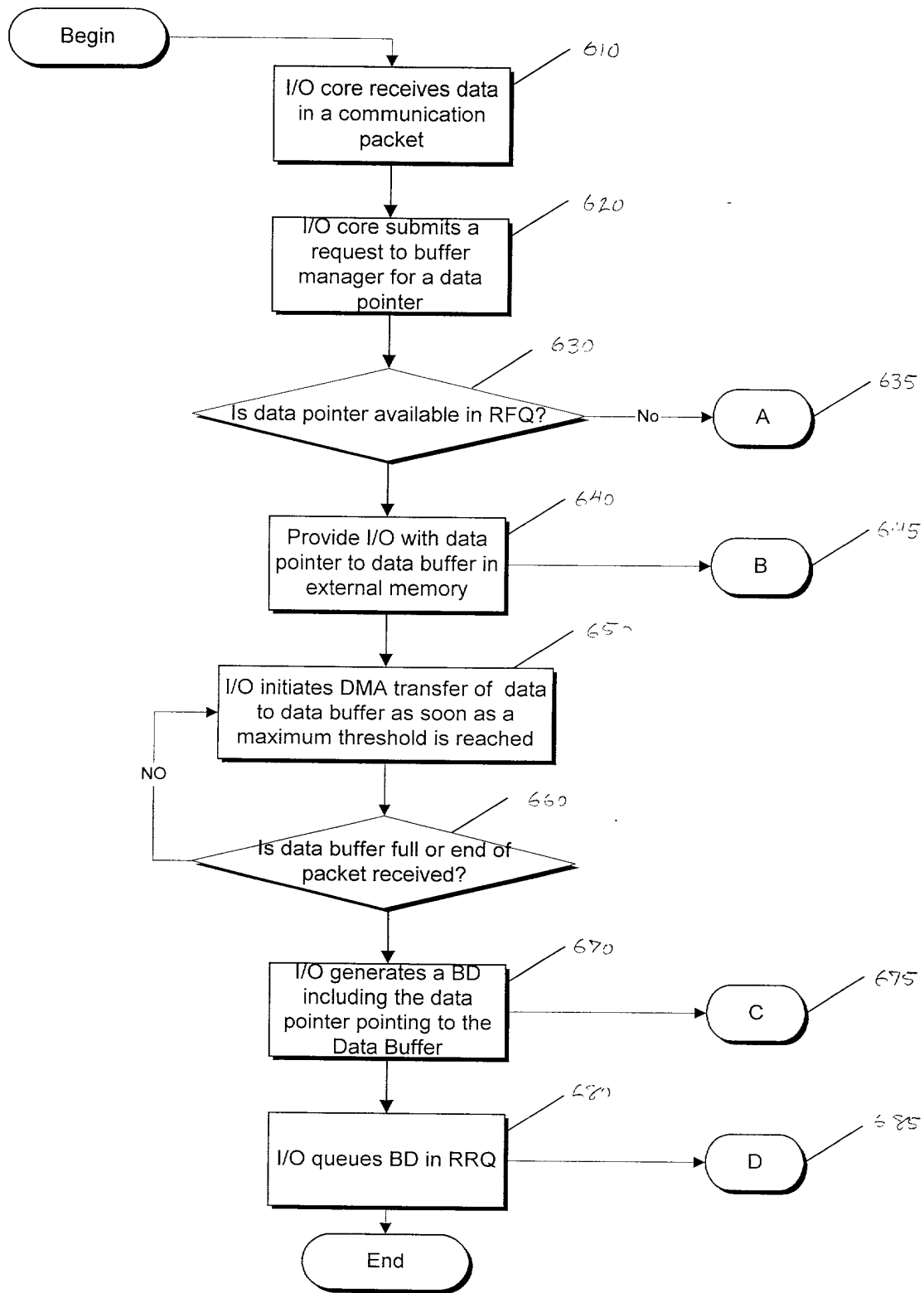


FIG. 6

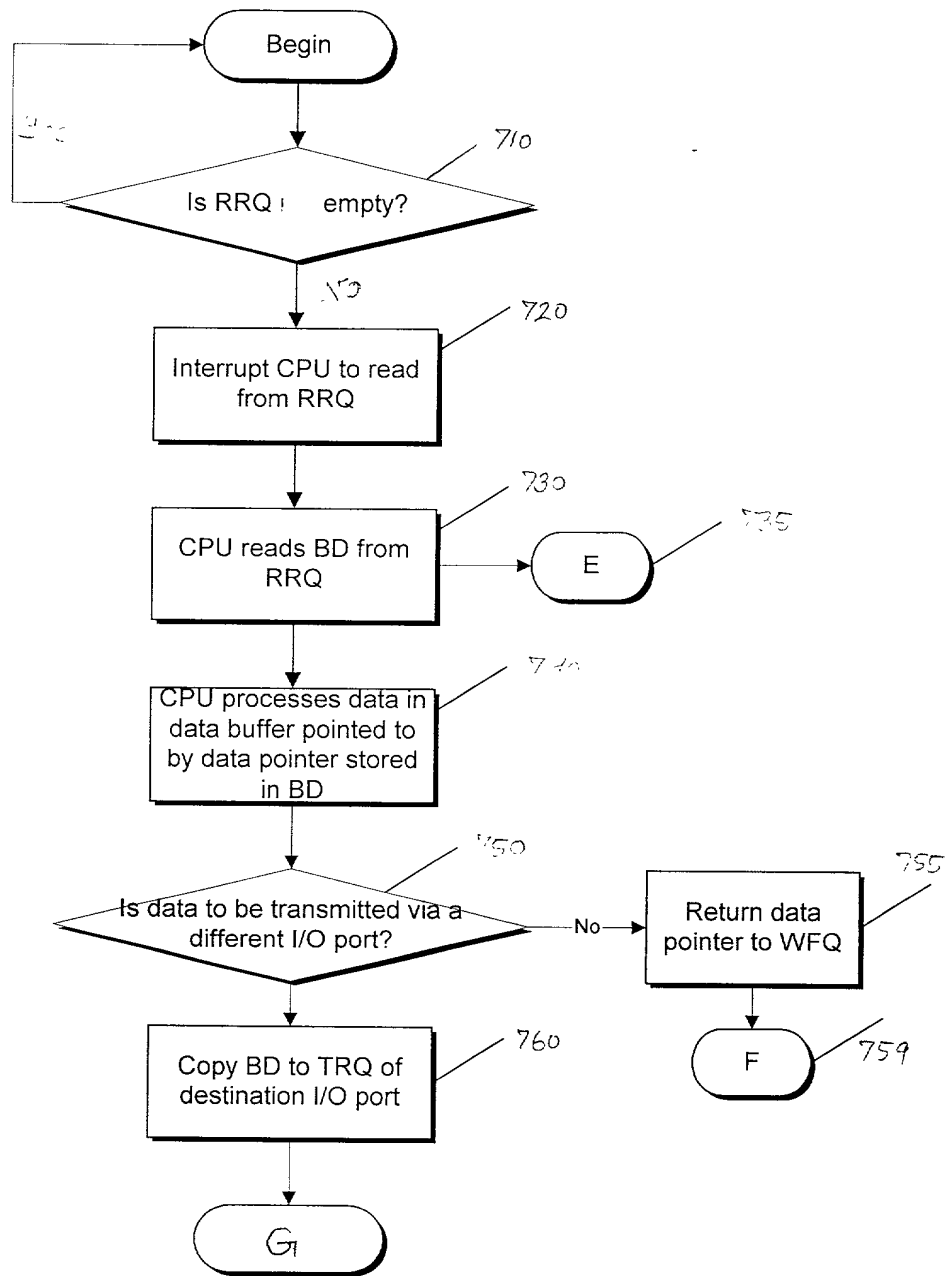


FIG. 7

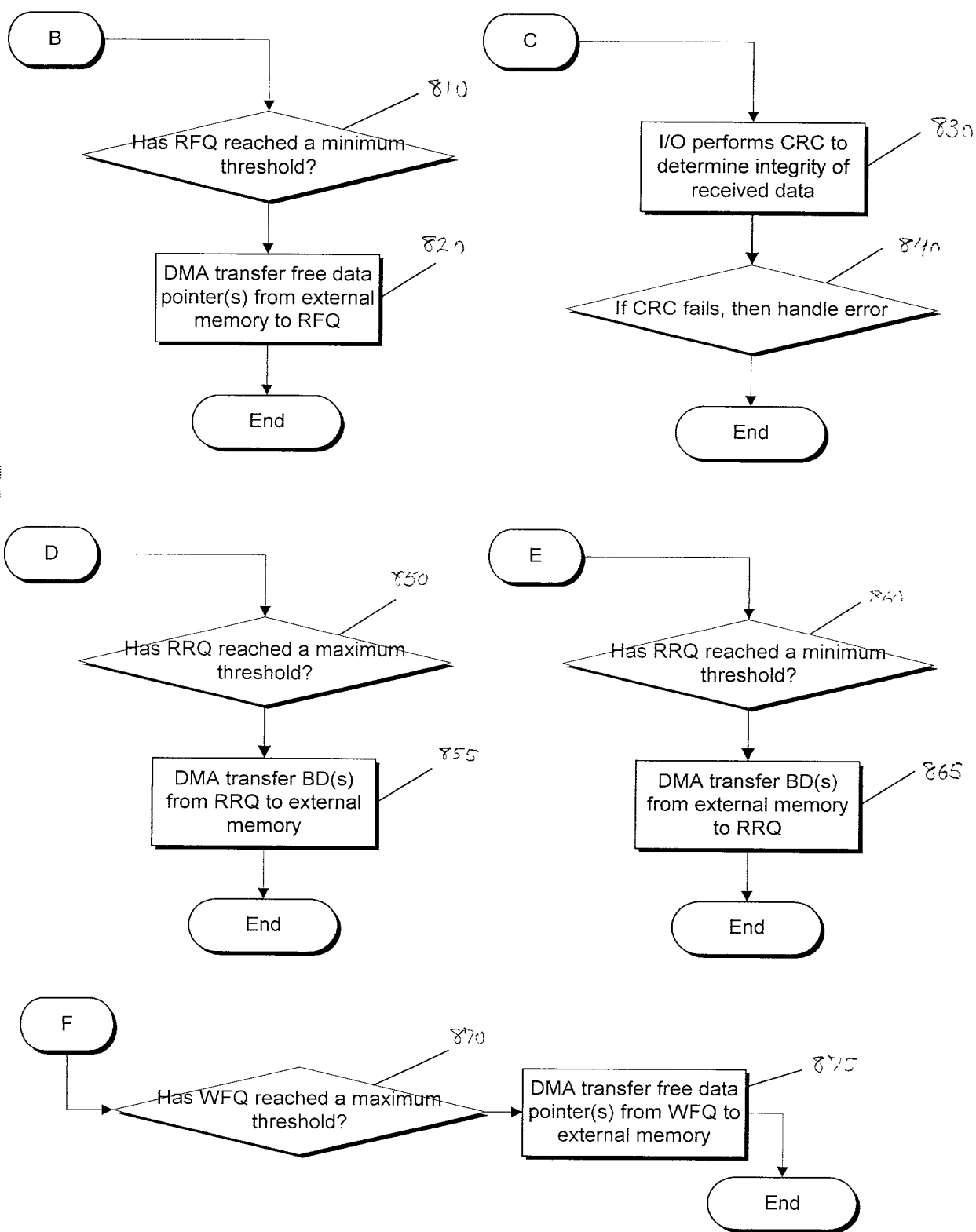


FIG. 8

FIG. 9

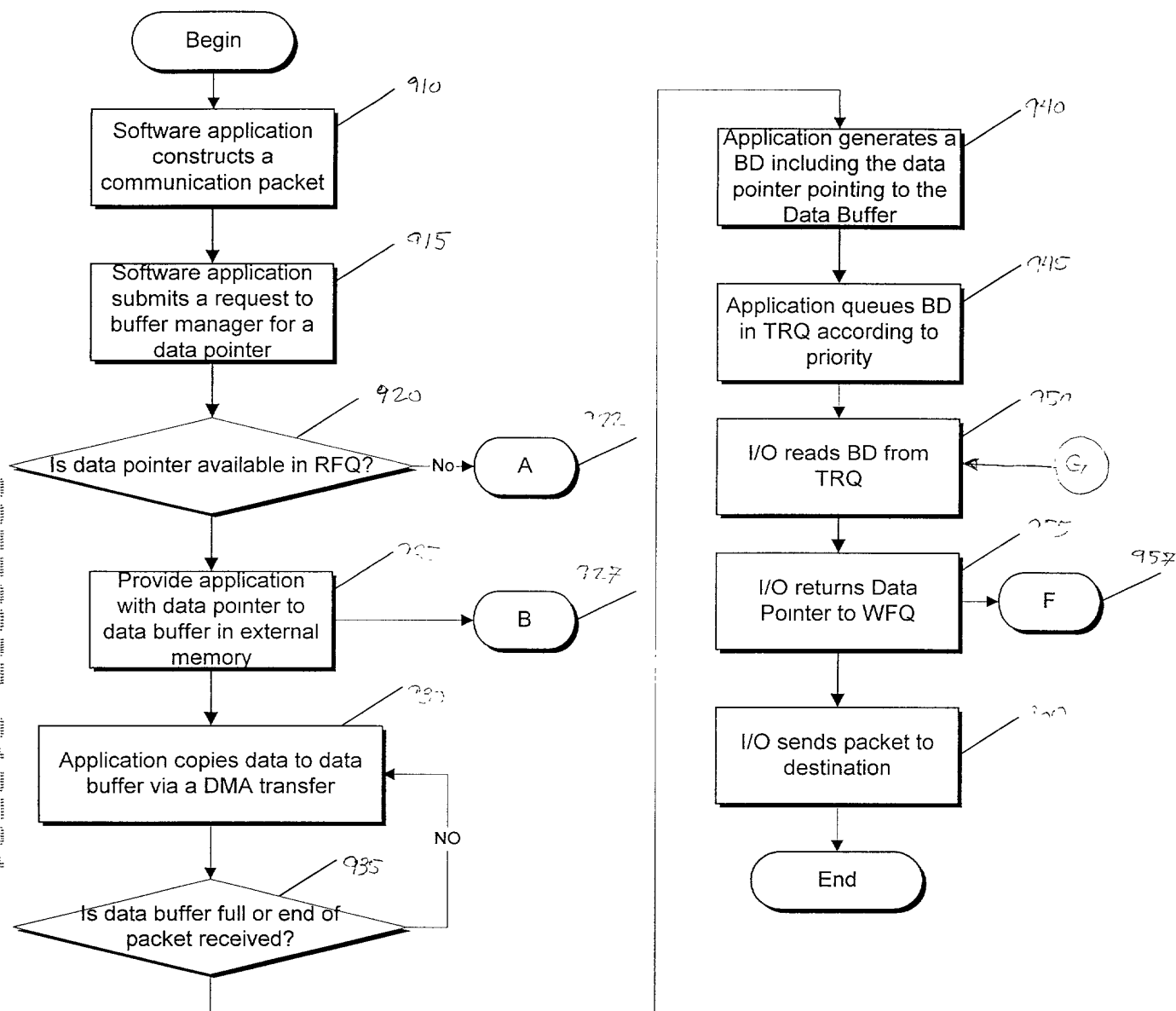


FIG. 9

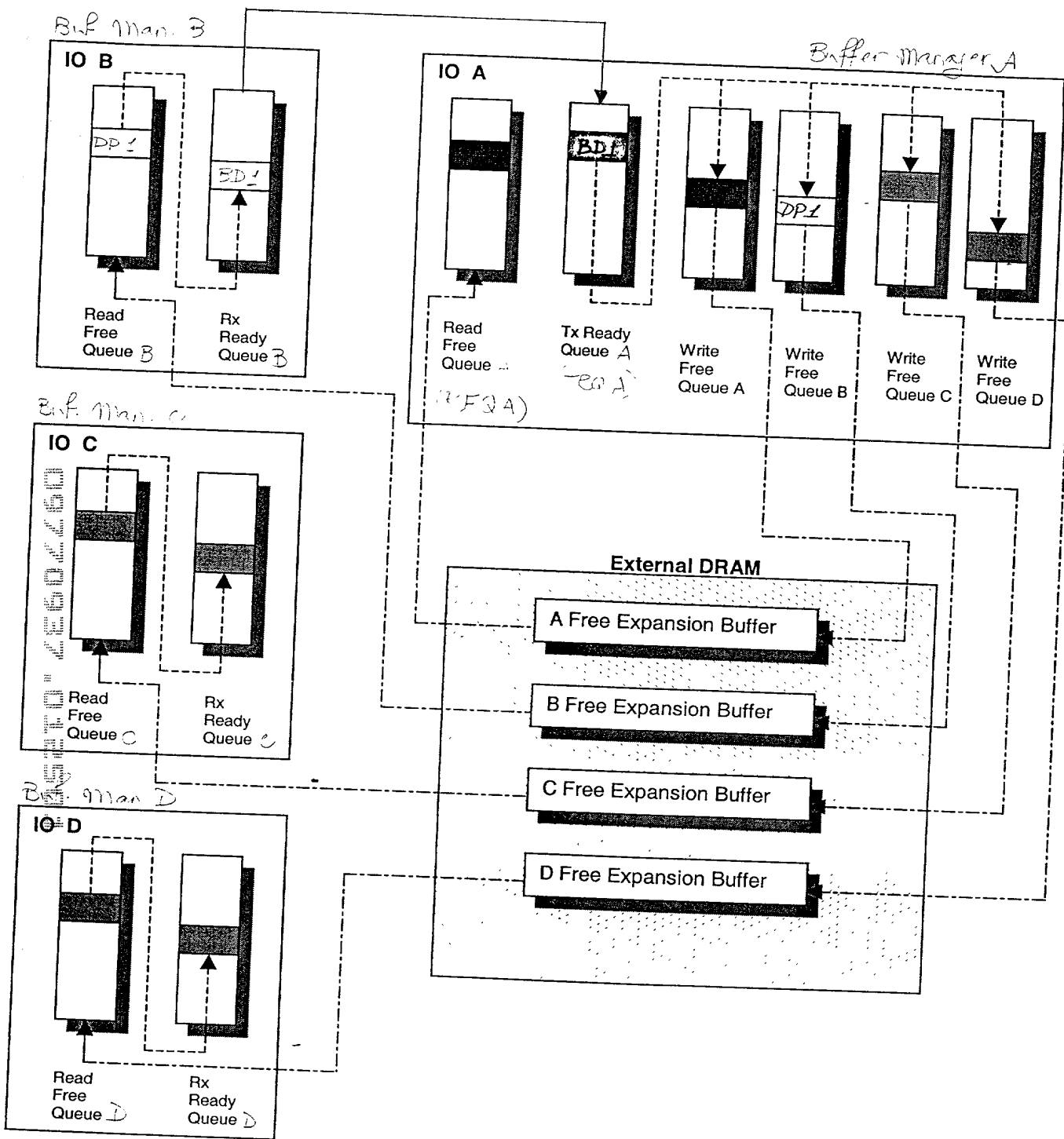


FIG. 10

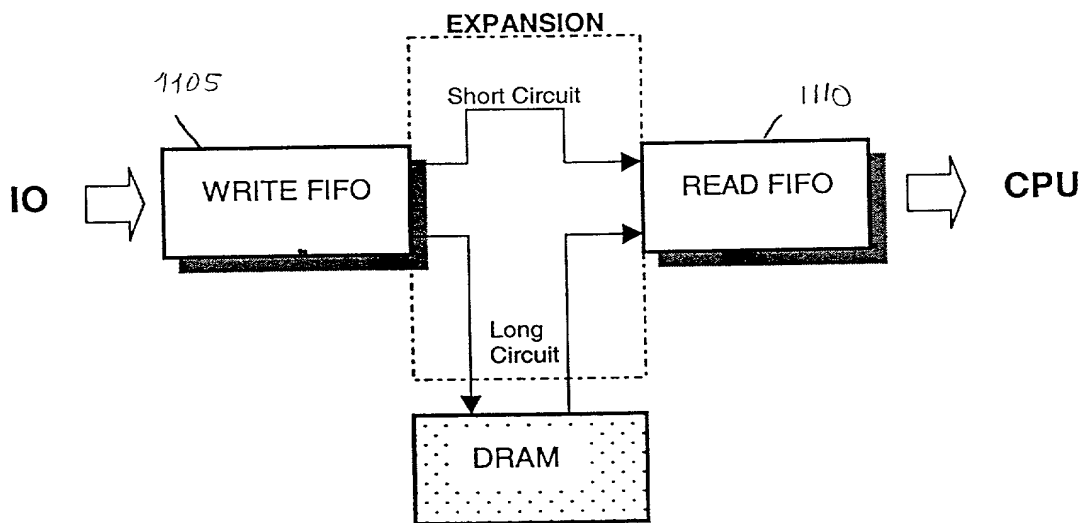


FIG. 11

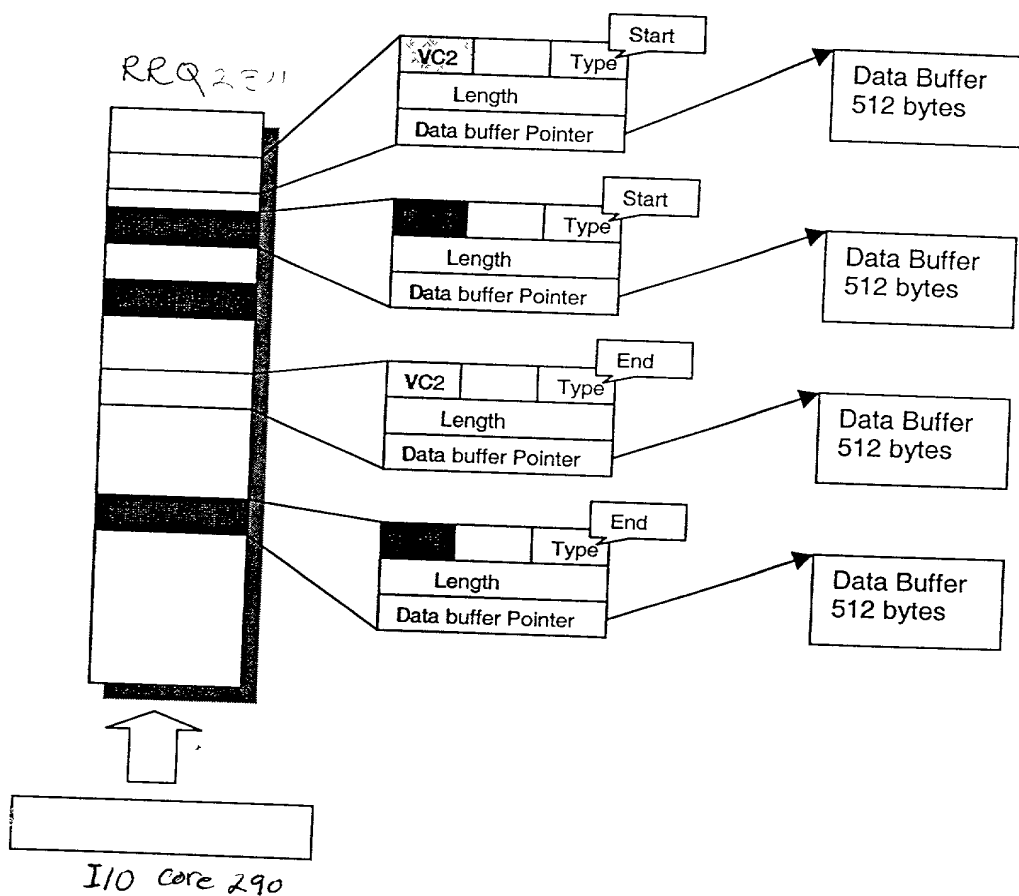


FIG. 12

109210-460460

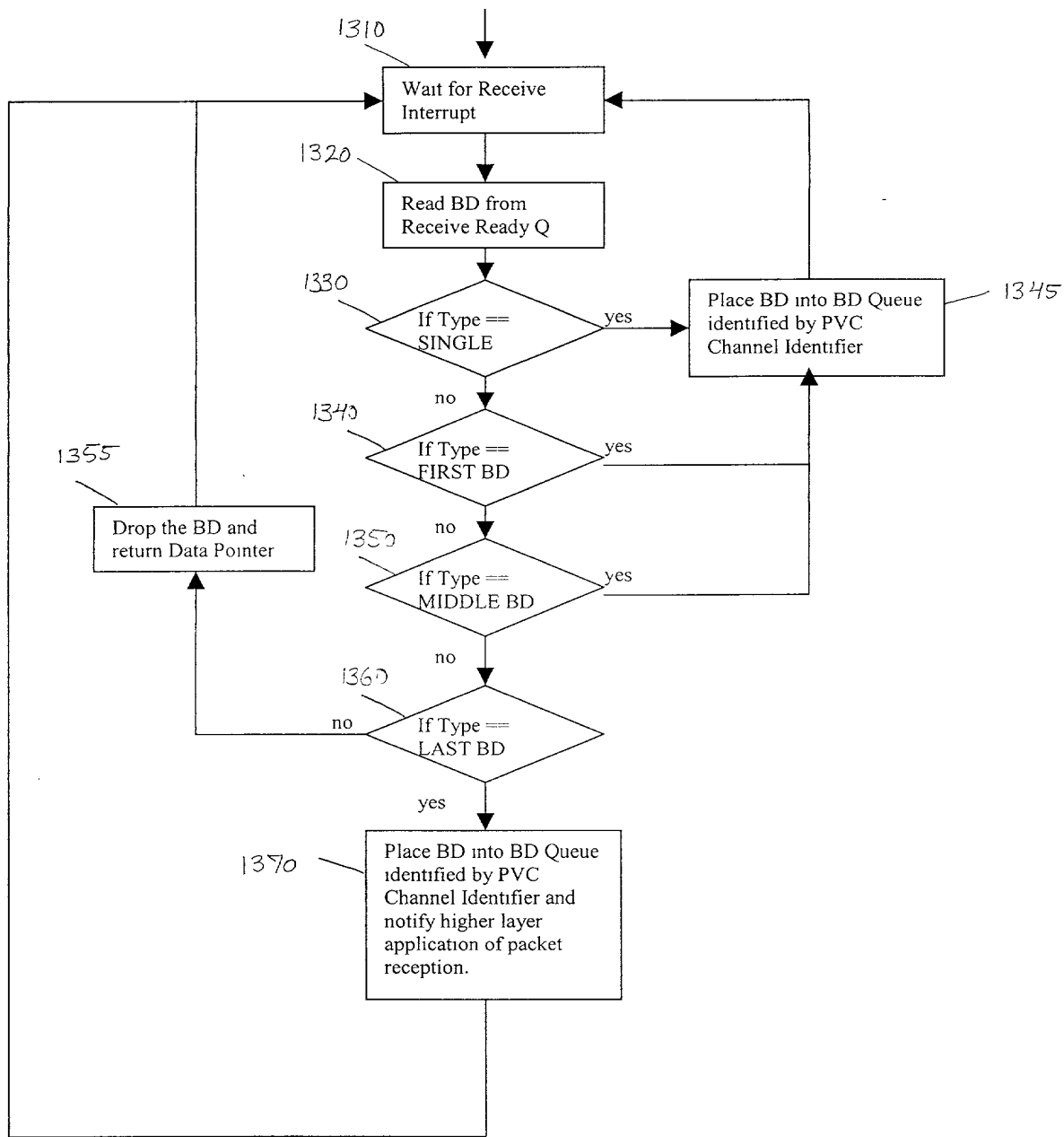


FIG. 13

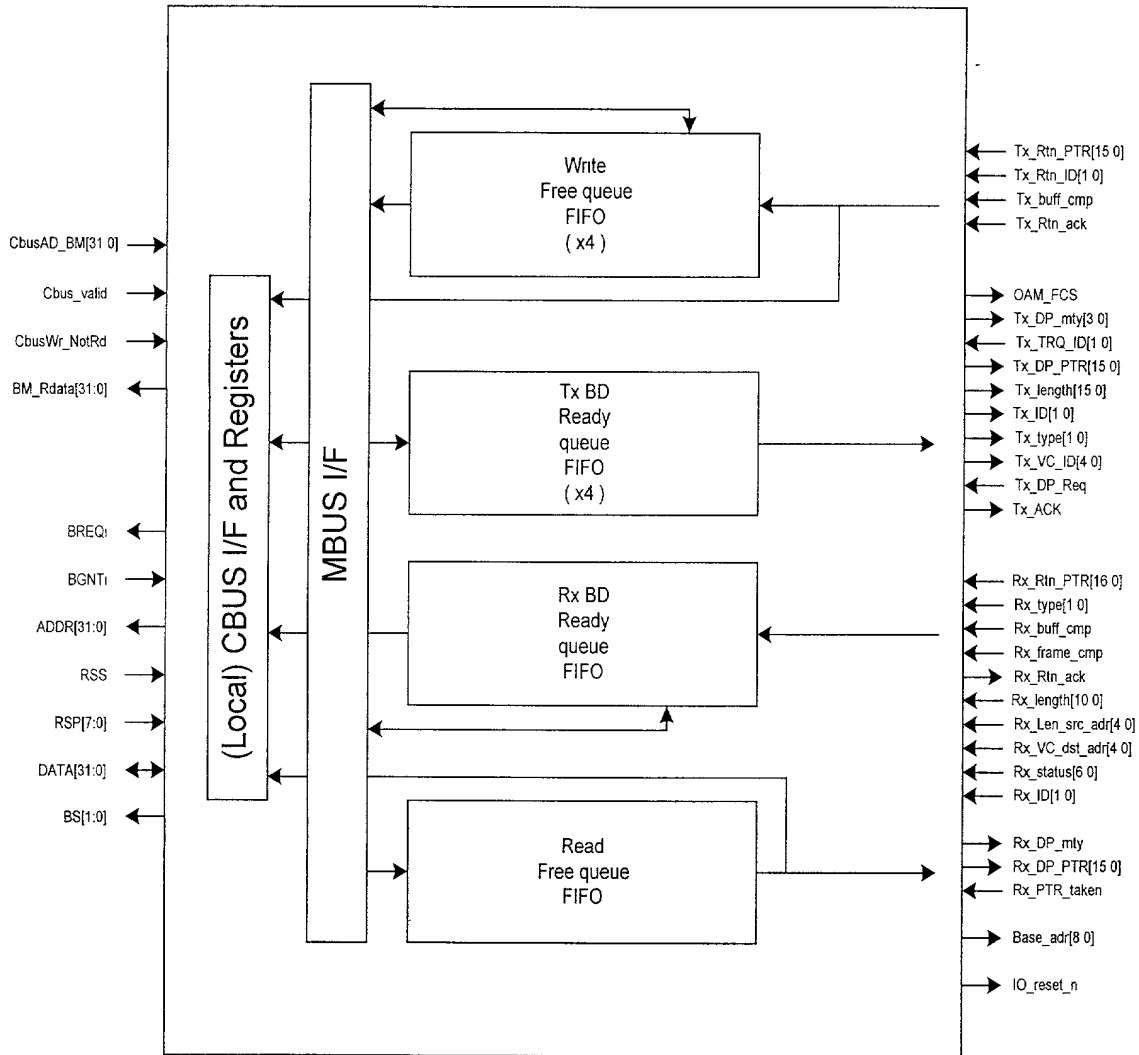


FIG. 14